Far-field RF Powering System for RFID and Implantable Devices with Monolithically Integrated On-Chip Antenna

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***Abstract* — A fully integrated far-field powering system for RFID and implantable devices with monolithically fully integrated on-chip antenna in 0.18µm CMOS is presented. The chip receives power, clock and data wirelessly through RF signal at all the three ISM bands of 915 MHz, 2.45 GHz and 5.8 GHz. Measurements show a minimum input power of -19.41 dBm at 900MHz for chip operation, corresponding to 15.7 meter of operation range with an off-chip 0dB gain antenna. On the other hand, with its on-chip antenna at 5.8 GHz, the chip can be powered-up up to 7.5 cm distance. This is a huge improvement in terms of operation distance compared with other reported similar works with on-chip antenna as well as the off-chip antennas.**

***Index Terms* — On-chip Antenna, OCA, RFID, Implantable, Wireless powering, far-field powering**

I. INTRODUCTION

While there have been real initial successes in the use of RFID technologies, the long-term potential benefits are immense. To date, RFID has demonstrated brighter prospects for companies wishing to gain process efficiency and transparency, as well as to identify additional business potential. Few examples of future substantial impact of RFID can be the advanced administration of healthcare services, pharmaceuticals, safety of bank notes and valuable documents. In all these applications, there may be a desire to implant the RFID chip into the target objects where size of the tag becomes very essential and determiner. The goal of this paper is to introduce our recent passive RFID chip with monolithically integrated On-Chip Antenna (OCA) on its top layer for these type of applications, where there is a huge improvement comparing to previously reported commercial and academicals works.

II. OPERATION PRINCIPLE

In general in the passive (battery-less) circuits the required power supply can be provided by any kind of energy sources such as thermal energy, vibration, movement, solar energy and so on. In our case, we use the electromagnetic energy of the incoming UHF wave at ISM frequencies of 900 MHz, 2.45 GHz or 5.8 GHz; for the latter this happens with an on-chip antenna where it enables the chip to be implanted in bank notes or any valuable document. For the uplink and data communication, usually backscattering or load modulation is used. However, the on-chip antenna low-gain reduces the operation distance significantly to a very close proximity. Therefore, an active transmitter can be used in uplink as a solution. However, the available power is too low to provide continuous powering for the circuitry operation; thus the tag captures energy for a longer time, rectifies it and stores it in a storage capacitor, and then uses this energy during the tag's operating period, hence duty cycling the tag's operation. As a result, the amount of available energy is limited and the tag's operation should be done in a time and power efficient approach. So for the uplink the Impulse UWB can be chosen for our system as a power-time efficient solution; this is discussed in more detail in our previous work at [7].In our system the powering-up signal is also used to carry the command and clock to the tags. Data and clock modulate the RF signal using Amplitude-Shift Keying (ASK) modulation with modulation depth from 30% to 100%. To realize the reception simply, binary data are encoded as pulse width modulation of the low-amplitude pulse such as conventional class 1 RFIDs. Time intervals for bit 1 are chosen to be 3 times of bit 0 (e.g. 1.5us for bit 0 and 4.5us for bit 1). A discriminator circuit in the tag will distinguish this difference and extract the 0s and 1s.

III. MONOLITHICALLY INTEGRATED ON-CHIP ANTENNA DESIGN

The most critical point of this design was the antenna as it directly determines the coverage distance. Targeting the standard CMOS technology and considering the very lossy silicon substrate,10 S/m conductivity, make the antenna design and considerations quite different with a normal antenna design. Simulations show that on such lossy substrates the antenna must meet the minimum required surface current path to have better efficiency (less loss) while at the same time needs to be conjugated matched to a capacitive impedance of the rectifier. In order to realize this a multi-turn loop-dipole structure with inductive and resistive stubs is developed and optimized

for this work. The antenna, shown in the die microphotographin of *Figure 4*, is less than 3X1.5 mm^2 in size and its IE3D and HFSS simulated realized-gain is around -29.5 dBi at 5.8 GHz.

IV. CIRCUIT IMPLEMENTATION

To demonstrate the proposed system concept, the module circuitry has been implemented in UMC 0.18µm CMOS.Figure 1 shows the detailed block diagram of the proposed module. It consists of a power management unit, an RF demodulator, a clock generator unit, and an on chip antenna for both short range wireless powering as well as data and clock. Unlike conventional passive tags where the incoming power is used directly for chip operation, here a different powering strategy has been used which reduces the required input power significantly. A power scavenging unit consisting of a chain of CMOS full-wave multiplier rectifies the incoming RF wave to DC voltage in an on-chip storage capacitor. Hence, the incoming power is accumulated in the storage capacitor and a low-power voltage sensor (Vsen) activates the chip when the voltage in the storage capacitor reaches an upper limit (V_H). The operation current is provided by discharging the storage capacitor down to the lower limit (V_L). Based on our simulation a minimum voltage of 1.2V is required for the transmitter to generate the desired pulse. Since the goal is to have the whole system on-chip so the storage capacitor size is an issue as well. Its size depends on the operation time, the required current consumption, and the difference between upper limit and lower limit as :

$$C = \frac{I\_time}{\Delta V} = \frac{I\_dc*(Rx\_time + Tx\_time) + I\_Tx*Tx\_time}{V_H - V_L}$$

Where I_dc is the current we estimate for baseband and other receiving blocks, I_Tx is the current of the transmitter and the clock generator (10uA at 1Mbps data rate based on our previous experiences and measurements), Rx_time is the receive time (around 200us i.e. 20 bits at 200Kbps). High upper limit reduces the required storage capacitor size, but it increases the required input power limiting the operational distance. On the other hand, choosing very low upper limit demand a large storage capacitor which occupies large area on-chip which is not feasible.

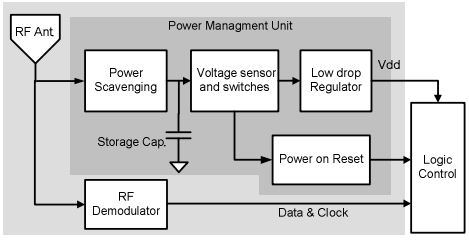

Figure 1: Block diagram of the proposed module

Based on our simulation the upper limit of 1.8V and a 6nF capacitor have been chosen. It can be implemented by MOSCAP which has higher capacity density. A low-drop-out (LDO) regulator provides a regulated voltage of 1.2V for the circuits A Power-on-Reset (PoR) circuit generates a reset signal for the logic control to eliminate the transient response of the Vsen and the LDO.

The operating distance of a chip depends on the efficiency of the power scavenging unit. A cross-connected CMOS full-wave multiplier is chosen here, since this architecture eliminate the threshold voltage of the transistor. Therefore, the required input voltage(power) would be less resulting longer operational distance.. The schematic of the power scavenging unit is shown in Figure 2. It includes a 9-stage full-wave voltage multiplier and a voltage limiter, which keeps the output voltage lower than the breakdown voltage. The goal is to design the rectifier able to produce 1.8V at the output and drive the Vsen with current of 330nA (i.e. 594nW)

The Vsen is the only operating part of the chip in the powering phase, therefore its static current is very critical. Figure 2 shows the schematic of the voltage sensor including a reference voltage generator, a Schmitt trigger comparator and a power switch. Having low power resistor-based bandgap references would need very big resistors, which occupy a large area [1]. Therefore, in this work a fully CMOS reference voltage is used [2]. A CMOS voltage divider divides the voltage across the storage capacitor and the comparator compares it with the reference voltage. The divider is designed to set the switch with 1.8 input voltage. As can be seen, the positive feedback through V2 changes the divider fraction. This changes the comparison voltage to 1.2V during discharging. It generates the 0.6 voltage range which provide the current needed for the chip operation.

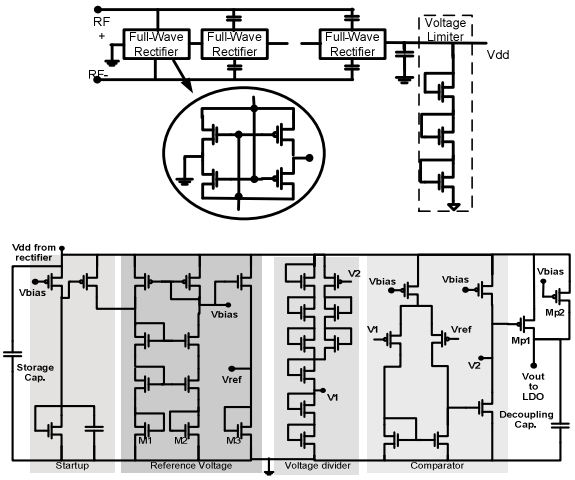

Figure 2: Schematic of the (a) power scavenging unit and (b)the voltage sensor

The schematic of the LDO is shown in Figure 3. The same reference voltage form the voltage sensor is used here. To reduce the power consumption, the bias current needs to be decreased which causes longer transient response for the LDO. In order to decrease the LDO's transient response, transistor MP2 in the voltage sensor provides a small bias current for the LDO circuitry during harvesting priod, which charges the LDO capacitors (parasitic and decoupling capacitors). This bias current can be very low hence does not affect the rectifier performance. In operation period MP1 is switched on and provides enough current for the LDO and the chip operation. Using this technique, can reduces the LDO's transient response significantly. The PoR circuitry is shown in Figure 3. A capacitor charged by a current source generates a pulse which is delayed compared to the signal from the Vsen.

The envelope detector is similar to the power scavenging unit structure but with only 2 stages. Figure 3 shows the block diagram of the RF demodulator including the envelope detector and a comparator circuitry. Q1 acts as an extra load for the envelope detector output which prevents generating high voltage when the incoming RF has higher levels. The extracted clock is used for data sampling and logic control; therefore no local oscillator is needed, which reduces the tag's power consumption significantly. The chip microphotograph is shown in Figure 4 and it occupies 4.5 mm^2.

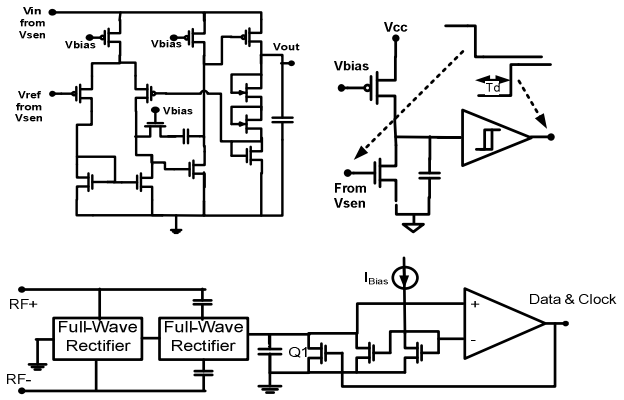

Figure 3: (a) Low-drop-out voltage regulator, (b) Power-on-Reset circuit and (c) RF demodulator

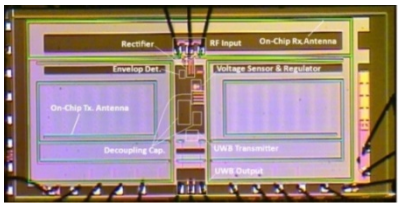

Figure 4: Die microphotograph

V. MEASUREMENT RESULTS AND DISCUSSION

To measure the input sensitivity of the power scavenging unit, the Rhode & Schwarz ZVM Network Analyzer has been used. The voltage sensor, the voltage regulator, and the power-on-reset are considered as the load of the power scavenging.

Measurement results have shown that as it was designed, the rectifier works for the all the 3 ISM bands of 900MHz, 2.45GHz and 5.8GHz while at the latter one the on-chip antenna are being used for short range power scavenging and data receiving. The input sensitivity at 900 MHz without on-chip antenna (having the antenna shoot out by the laser machine) has been measured to be -19.41 dBm by direct probing the chip. Considering 36 dBm EIRP radiation and an external 0 dB gain receive antenna, this corresponds to a 15.7 meter powering distance, which is a great improvement compared to existing passive RFIDs [3]. This improvement is due to the use of the voltage sensor and duty cycling the operation, which reduces the power consumption during harvesting improving the input sensitivity. To occupy a small area, the on-chip antenna has been designed at 5.8 GHz. A wireless operational distance of 7.5cm is achieved under 36 dBm EIRP, which is a huge improvement compared with previously reported works [4-6].

Figure 5.a shows the frequency response of the wireless powering. As can be seen, the chip can operate in a wide range of the frequency band. It can help the chip works when present any frequency shift due to proximity or any unexpected variation. Figure 5.b depicts the rectified voltage versus distance for different extra loads at the rectifier output. It confirms that having circuit with less current consumption longer operational distance can be achieved. Figure *6*.a shows the rectifier output voltage across the storage capacitor and the PoR signal. As can be seen the upper and lower limit is measured to be 2V and 1.3V respectively. The deviation from the simulation results is due to the process variation. However this variation does not affect the circuit operation but increment in upper limit reduces the operational distance.

An ASK-modulated RF signal as explained before has been used to measure the data and clock recovery performance. The measurement result at 500 kHz clock is shown Figure 6.b. Higher clock could not be measured because of the instrument limitation in our lab.

Table 1 summarizes and compares the measurement results with three other related works.

VII. CONCLUSION

A fully integrated far-field powering system for RFID and implantable devices with monolithically fully integrated on-chip antenna in 0.18µm CMOS is presented. Measurement results confirm that the chip can be powered up at all the three ISM bands of 915 MHz, 2.45 GHz and 5.8 GHz. In order to minimize the power consumption the chip receives its clock and the commands wirelessly through the modulated RF powering-up signal. Measurement results show that the chip can operate with a minimum input power of -19.41 dBm at 900MHz band, corresponding to 15.7 meter of operation range with assuming an off-chip 0dB gain antenna. On the other hand, with the implemented on-chip antenna at the top layer at the 5.8 GHz band, the chip can be powered up up to 7.5 cm distance. This is a huge improvement in terms of operation distance compared with other reported similar works with on-chip antenna as well as the off-chip antennas.

Table 1: Summary of measurement results

		This work	[4]	[7]
Technology		0.18µm	0.18µm	0.18µm
Die area(mm^2)		4.5	0.6	4.5
Frequency		900 MHz, 2.45 &5.8	900MHz	900MHz
Input sensitivity (dBm)	900 MHz	-19.41	-	-18.5
	2.45 GHz	-16.2	-	-
	5.8G Hz	-14.22 dBm	-	-
Vout/I (µA)		1.8 V/0.33	1 V/10	2.7V/1.5
Distance with off-chip antenna	900 MHz	15.7 meter	-	13.9 m
	2.45 GHz	4 meter		-
	5.8 GHz	1.5 meter		-
Distance with OCA		7.5cm (4W EIRP/5.8G	4 mm	-
Need for off-chip component		No off-chip component	-	Antenna & storage capacitor

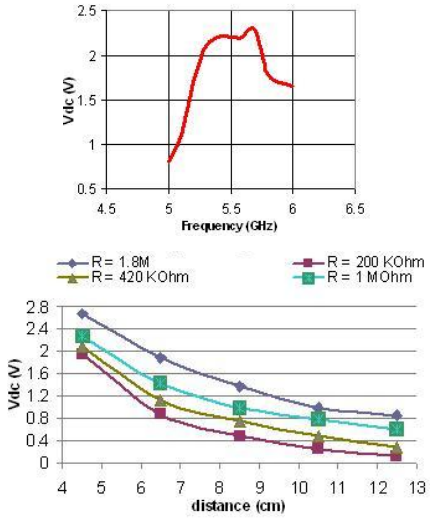

Figure 5: a) Frequency response of wireless powering and b) the wireless powering response versus distance

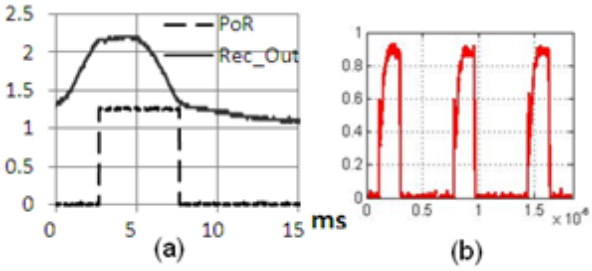

Figure 6: a) Rectifier output charge/discharge and Power-on-Reset output waveforms, b) Measurement result for the ASK demodulator

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